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06CS33

Third Semester B.E. Degree Examination, January 2013
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Realize XOR gate using NAND gates. **(06 Marks)**

b. Obtain minimal expression from the following SOP using K-map method
$f(A, B, C, D) = \sum m(1, 4, 5, 6, 7, 10, 11, 13) + \sum d(9, 3, 14)$. **(07 Marks)**

c. Obtain minimal expression from the following SOP using Quine Mc Cluskey's method.
$F(A, B, C, D) = \sum m(1, 3, 4, 5, 6, 7, 13, 15)$. **(07 Marks)**

2 a. Realize 4:1 MUX using verilog HDL. **(06 Marks)**

b. Write circuit diagram and explain the BCD – To – Decimal decoder. **(07 Marks)**

c. Explain odd parity generation with the help of diagram. How do you convert it to even parity generator. **(07 Marks)**

3 a. Write verilog HDL program for full adder. **(05 Marks)**

b. Write circuit diagram of 4-bit parallel adder/subtractor circuit and explain. **(07 Marks)**

c. What are fast adders? Draw and explain 2-bit fast adder circuit diagram. **(08 Marks)**

4 a. Realize the edge triggered flip-flop of JK type using verilog HDL. **(06 Marks)**

b. Write the conversion procedure for converting RS flip-flop to JK flip-flop. **(07 Marks)**

c. Derive the characteristic equation for SR flip-flop. **(07 Marks)**

PART – B

5 a. Realize 4-bit shift right register using verilog HDL. **(06 Marks)**

b. Explain SIPO register configuration with the help of diagram and sequence table (state table) or waveforms. **(07 Marks)**

c. Realize 3 bit up-down asynchronous counter with the help of flip-flop and explain. **(07 Marks)**

6 a. Write and briefly explain Melay and Moore models in sequential logic system. **(04 Marks)**

b. Write Melay state transition diagram, state table, k-maps and the circuit diagram for detection of three-bit sequence 110. **(10 Marks)**

c. i) What is an ASM chart?
ii) Discuss the problems related to asynchronous sequential circuits. **(06 Marks)**

7 a. Explain 4-stage R-2R ladder circuit used for A-D conversion, calculate its resolution. **(10 Marks)**

b. Write a block diagram to explain counter method A/D conversion. **(10 Marks)**

8 a. Explain TTL NAND gate circuit diagram. Verify the circuit diagram with reference to Nand gate truth table. **(08 Marks)**

b. Discuss TTL-to-CMOS and CMOS-to-TTL interface. **(08 Marks)**

c. Write notes on switching circuits. **(04 Marks)**

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